REMARKS

The above Amendments and these Remarks are in reply to the Office Action mailed July 2, 2003. Claims 1-51 are pending in the application. Claims 1, 5-7, 12, 14, 23-24, 29, 32-34, and 42 have been amended and claims 45-51 have been added. Applicant asserts that claims 1-51 are in condition for allowance and respectfully requests consideration of these claims.

I. Amendments to the Specification

Applicant has amended the brief description of FIGS. 2-5 on page 6 of the Specification to more accurately and clearly describe the contents of these figures. No new matter has been added by these amendments.

II. Amendments to claims 5-7, 24, 32, 33

Claims 5-7, 24, and 32-33 have been amended to correct minor typographical errors. These amendments are not made for any reason related to patentability or in response to any rejection or objection issued by the Examiner.

III. Objections to the Drawings

A. FIGS. 2-5

The Examiner objected to FIGS. 2-5 stating that the labels for FIGS. 2 and 4, and FIGS. 3 and 5, respectively, appear to have switched. Applicant asserts that no drawing correction to these figures is required for the reasons set forth below.

Applicant has amended the brief description of FIGS. 2-5 on page 6 of the Specification to clarify that these figures illustrate memory models. The labels on FIGS. 2 (MEMORY WRITE) and 3 (MEMORY READ) indicate that the memory models depicted therein are for a memory write operation and a memory read operation, respectively. Accordingly, Applicants assert that no correction to these drawings is required. The labels on the figures is accurate and properly describes a portion of the figures' contents.

The descriptions of FIGS. 4 and 5 have been amended to clarify that these figures are flowcharts. FIGS. 4 and 5 do not include labels. Accordingly, Applicant asserts that no drawing correction with respect to FIGS. 4 and 5 is required.

Applicant respectfully requests withdrawal of the Examiner's objection to FIGS. 2-5.

B. FIG. 6

The Examiner objected to FIG. 6, asserting that "[a] Fig. 6 is listed in the specification (p. 6), yet none has been provided." *Office Action*, p. 2, para. 2. Applicants, however, respectfully submit that a FIG. 6 was included in the original filing of the present application. Applicants filing papers included 8 pages of drawings. The pages included a page each for FIGS. 1-6, a page for FIGS. 6A&B, and a page for FIG. 7. A copy of the application transmittal form is included as Attachment B to this response and indicates the inclusion of 8 pages of drawings with the application filing. A copy of a postcard included with the application filing and listing 8 pages of drawings as part of the filing is included as Attachment C to this response. The postcard includes a stamp from the USPTO dated June 2, 2000 that indicates receipt of the postcard and the items listed thereon. Thus, FIG. 6 has been provided to the USPTO as indicated by the date stamp.

Accordingly, Applicants assert that no drawing correction with respect to FIG. 6 is required. A copy of FIG. 6 as originally filed is included as Attachment A to this response. A second courtesy copy of FIG. 6 is also included herewith for the convenience of the Examiner.

IV. Rejection of Claims 1-22 and 29-44 under 35 U.S.C. § 102(b)

Claims 1-22 and 29-44 were rejected under 35 U.S.C. § 102(b) as being anticipated by Weems, Charles C. Jr., "CmpSci 535 Notes from Lecture 9: Memory Hierarchy and Caching." (*Weems*). Applicant asserts that *Weems* fails to disclose each of the limitations of claims 1-22 and 29-44 and thus, does not anticipate these claims.

Embodiments of the present invention relate to memory modeling for use with electronic design automation (EDA) tools. This memory modeling for use with EDA tools is performed prior to the development of any actual physical memory or physical circuit. In one embodiment for example, an EDA tool that can exclusively be software, is used to model, synthesize, and/or simulate a circuit design model described only in a software language such as hardware description language (HDL) or by a gate level netlist. No hardware is needed to perform the modeling or to describe the electronic circuit design. Accordingly, the EDA tools permit "designers to more quickly and inexpensively design and verify their designs" before a routing software package is used to complete an actual physical design. *See generally, Specification*, pp. 1-2. Prior art memory models suffered from the disadvantages of modeling "every location of the

memory" and only functioning "with simulation or verification engines of the same vendor" as the EDA tools. *Id.* at p. 3, l. 14 – p. 4., l. 1.

One embodiment of the present invention addresses the problems with prior art memory models by providing a "method for modeling a physical memory for use in an electronic circuit design where memory write operations to the physical memory and memory read operations from the physical memory are modeled in a lookup table." *Id.*, p. 4, ll. 12-15. Claim 1, for example, recites modeling memory operations in a lookup table "wherein the lookup table is used to represent the physical memory with a description of the electronic design."

In contrast to Applicant's claimed invention, *Weems* is directed to memory hierarchy and caching and provides an overview of traditional caching techniques and related methodologies in actual physical systems including multiple types of memory. The discussion in *Weems* is directed to traditional caching techniques and physical cache memory such as those that "use a small amount of very fast memory to effectively accelerate the majority of memory accesses." *Weems*, p. 2. Accordingly, *Weems* discloses an overview of memory caching using various actual memories, but does not disclose or suggest anything relating to modeling physical memories in an electronic design through the use of a lookup table or otherwise.

A. Claims 1-11

Because Weems does not disclose each of the limitations of claim 1, Applicant asserts that claim 1 is patentable over the cited art. Claim 1 recites "modeling a memory write operation using a lookup table; and modeling a memory read operation using the lookup table; wherein the lookup table is used to represent the physical memory with a description of the electronic design." The process of simulating/verifying an electronic circuit design can begin with the creation of a circuit description of the design. *See Specification*, p. 13, ll. 21-23. In one embodiment of the present invention, after reducing the circuit description to a gate level description of the electronic circuit design, "that portion of the gate level description 640 relating to the physical memory is then replaced with lookup table 645 wherein lookup table 645 effectively models all read and write ports of the physical memory." *Id.* at p. 14, ll. 1-10.

Weems is not concerned with and does not disclose modeling any memory operations or using a lookup table "to represent the physical memory with a description of the electronic design," as recited in claim 1 (*emphasis added*). *Weems* merely discusses the concept of using

physical instruction and/or memory caches in computer systems utilizing main memories and secondary memories to "end up with a system that can hold a large amount of information (in a large, low-cost memory) yet provide nearly the same access speed as would be obtained from having all of the memory be very fast and expensive." *Weems*, p. 2.

The Figure on p. 3 of *Weems*, as cited by the Examiner, is merely a diagram of a cache that contains "lines of data, usually containing values from two or more consecutive addresses of main memory. Each line has associated with it a tag that stores the high order bits of the addresses in the line." *Id.* at p. 3. If there is a match when in the cache when a memory reference occurs, the line of data is read from the cache. Nothing within the text associated with the Figure on p. 3 discloses modeling memory operations using a lookup table or "wherein the lookup table is used to represent the physical memory with a description of the electronic design," as recited in claim 1. *Weems* is not directed to and does not discuss lookup tables for representing physical memories in descriptions of electronic designs.

Pages 7-8 of *Weems* (Write and Write Buffer as cited by the Examiner) similarly do not discuss the limitations of claim 1. With regards to writing a value to the cache, *Weems* discloses the techniques of "write through" whereby "we can write it to the cache and simultaneously write it in through to the main memory," and "write back" whereby "we can write it to the cache and not write it back to the main memory until it is replaced." *Id.* at p. 7. A write buffer as described by *Weems* is a small set of registers to which "data and its destination address are written ... where they waits for memory to become available so the data can actually be stored." *Id.* at p. 8.

Thus, *Weems* is directed to and discloses the use of memory caching and related techniques in actual physical systems to improve performance by maintaining some amount of information in a faster memory. There is nothing within *Weems* to suggest the use of lookup tables that can be used to represent physical memories with a description of an electronic design. *Weems* provides no discussion of electronic circuit design, nor the use of lookup tables in representing portions of electronic designs. Accordingly, nothing within *Weems* discloses or suggests "modeling a memory write operation using a lookup table," "modeling a memory read operation using the lookup table," or "wherein the lookup table is used to represent the physical memory with a description of the electronic design," as recited in claim 1.

Because *Weems* does not disclose each of the limitations of claim 1, Applicant asserts that claim 1 is patentable over the cited art. Claims 2-11 each ultimately depend from claim 1, and

should be patentable over the cited art for at least the reasons set forth above with respect to claim 1. Accordingly, Applicant respectfully requests withdrawal of the rejection of claims 1-11 under 35 U.S.C. § 102(b).

B. Claims 12-13

Because *Weems* does not disclose each of the limitations of claims 12-13, Applicant asserts that claims 12-13 are patentable over the cited art.

Claim 12 recites "initializing the lookup table, wherein the lookup table is used to represent the combinational block with a description of the electronic circuit design." As described in Applicant's Specification, "the lookup table of the present invention can be used to model so called 'black boxes' or uninterpreted portions of a design." *See Specification*, p. 15, ll. 8-9. As discussed above with respect to claim 1, *Weems* does not disclose or suggest the use of a lookup table to "represent the physical memory with a description of the electronic design." Similarly, *Weems* does not disclose or suggest the use of a lookup table "to represent the combinational block with a description of the electronic circuit design," as recited in claim 12. *Weems* is concerned exclusively with caches and memory hierarchy and does not discuss descriptions of electronic circuits and their designs. Accordingly, nothing within *Weems* suggests or discloses the use of lookup tables to represent combinational blocks with descriptions of electronic circuit designs.

Pages 3-6 of *Weems*, as additionally cited by the Examiner, discuss various implementation schemes of caches and replacement policies used in some schemes. For example, *Weems* discusses fully associative and direct-mapped caches. Nothing within this section of *Weems* is directed to a lookup table to "represent the combinational block with a description of the electronic circuit design," as recited in claim 12. "Paging" and the "presence bit" in the top Figure on p. 11 of *Weems* also fail to discuss the above limitations of claim 12. As described in *Weems*, paging is used with virtual memory such that, "[m]emory is divided into fixed-size blocks called pages." *Weems*, p. 11. Virtual memory is defined by *Weems* as a "mapping from a virtual address space to a physical address space," or a "mapping from a name space to an address space." *Id.* at p. 10. "In order to perform the mapping function, a table lookup is performed." *Id.* at p. 11. The lookup table of *Weems* is used for performing a mapping function for a physical address space, not for "representing the combinational block with a

description of the electronic circuit design," as recited in claim 12 (*emphasis added*). Furthermore, the presence bit of *Weems* merely "indicates whether the physical page is in main memory or must be fetched from secondary storage (a page fault)." *Id.*

Nothing within any of the cited portions of *Weems* discloses or suggests "initializing the lookup table, wherein the lookup table is used to represent the combinational block with a description of the electronic circuit design," as recited in claim 12. Because *Weems* does not disclose each of the limitations of claim 12, Applicants assert that claim 12 is patentable over the cited art. Claim 13 depends from claim 1, and should be patentable over the cited art for at least the reasons set forth above with respect to claim 12. Accordingly, Applicants respectfully request withdrawal of the rejection of claims 12-13 under 35 U.S.C. § 102(b).

C. Claims 14-22

Because *Weems* does not disclose each of the limitations of claims 14-22, Applicant asserts that claims 14-22 are patentable over the cited art.

Claim 14 recites "modeling a memory write operation in a memory model to represent a memory write operation in the physical memory, the memory is model used to represent the physical memory with a description of the electronic circuit design." As discussed above, nothing within *Weems* discloses or suggests "wherein the lookup table is used to represent the physical memory with a description of the electronic design," as recited in claim 1, or "initializing the lookup table, wherein the lookup table is used to represent the combinational block of the electronic circuit design with a description of the electronic circuit," as recited in claim 12. As with a lookup table, nothing within *Weems* discloses or suggests a "memory model is used to represent the physical memory with a description of the electronic circuit design." *Weems* merely discusses caching in physical systems utilizing multiple memories. *Weems* is not directed to electronic circuit designs and provides no discussion of using a "memory model to represent the physical memory with a description of the electronic circuit design," as recited in claim 14.

Because *Weems* does not disclose each of the limitations of claim 14, Applicant asserts that claim 14 is patentable over the cited art. Claims 15-22 each ultimately depend from claim 14, and should be patentable for at least the reasons set forth above with respect to claim 14.

Accordingly, Applicant respectfully requests withdrawal of the rejection of claims 14-22 under 35 U.S.C. § 102(b).

D. Claims 29-33

Because *Weems* does not disclose each of the limitations of claims 29-33, Applicant asserts that claims 29-33 are patentable over the cited art. Claim 29 recites, a processor readable storage medium including code "for programming a processor to perform a method for creating a memory model for use in modeling an electronic circuit design having a physical memory," and "wherein the lookup table is used to represent the physical memory with a description of the electronic circuit design."

Thus, for the reasons set forth above with respect to claim 1, Applicants assert that claim 29 is patentable over the cited art. Claims 30-33 each ultimately depend from claim 29, and should be patentable over the cited art for at least the reasons set forth above with respect to claim 29. Accordingly, Applicants respectfully request withdrawal of the rejection of claims 29-33 under 35 U.S.C. § 102(b).

E. Claims 34-41

Because *Weems* does not disclose each of the limitations of claims 34-41, Applicant asserts that claims 33-41 are patentable over the cited art. Claim 34 recites, "wherein the memory model is used to represent the physical memory with a description of the electronic circuit design." Thus, for the reasons set forth above with respect to claims 1 and 14, Applicants assert that claim 34 is patentable over the cited art. Claims 35-41 each ultimately depend from claim 34, and should be patentable over the cited art for at least the reasons set forth above with respect to claim 34. Accordingly, Applicants respectfully request withdrawal of the rejection of claims 34-41 under 35 U.S.C. § 102(b).

F. Claims 42-44

Because *Weems* does not disclose each of the limitations of claims 42-44, Applicant asserts that claims 42-44 are patentable over the cited art. Claim 42 recites, "wherein the lookup table is used to represent the uninterpreted combinational block with a description of the electronic circuit design." Thus, for the reasons set forth above with respect to claims 1 and 12,

Applicants assert that claim 42 is patentable over the cited art. Claims 43-44 each ultimately depend from claim 42, and should be patentable over the cited art for at least the reasons set forth above with respect to claim 42. Accordingly, Applicants respectfully request withdrawal of the rejection of claims 42-44 under 35 U.S.C. § 102(b).

V. Rejection of Claim 23 under 35 U.S.C. § 102(b)

Claim 23 was rejected under 35 U.S.C. § 102(b) as being anticipated by Bayoumi, M. et al., "A look-up table VLSI design methodology for RNS structures used in DSP applications," IEEE Transactions on Circuits and Systems, Vol. 34, Issue 6, June 1987, pp. 604-616 (*Bayoumi*). Because *Bayoumi* does not disclose each of the limitations of claim 23, Applicant asserts that claim 23 is patentable over the cited art.

Claim 23 recites "creating the lookup table, the lookup table having a total number of entries that is greater than or substantially equal to an upper limit, the lookup table representing the physical memory with a description of the electronic circuit design." *Bayoumi*, however, is directed to a design methodology for Residue Number System (RNS) structures based on using look-up tables. The method described in *Bayoumi* develops a look-up table layout model and selects the most efficient layout according to the design requirements by allowing the designer to control the area, time, or the configuration of the memory module required for implementing a modulo look-up table. *See Abstract*, p. 604. While *Bayoumi* discusses look-up tables, the look-up tables are used to store the RNS structures, not to "represent the physical memory with a description of the electronic circuit design," as recited in claim 23.

Bayoumi describes a look-up table layout methodology "based on developing a realization (physical) model for the layout of the memory module." *Bayoumi*, p. 606. After developing a memory model, the look-up table layout procedure is performed whereby "[t]he layout of a memory module for storing a modulo *m* look-up table is controlled by the following features." *Id.* at p. 608. Thus, *Bayoumi* is directed to and discloses the development of a look-up table layout model and memory modules for storing look-up tables required for RNS structures. Nothing within *Bayoumi*, however, discloses or suggests the use or development of lookup tables to represent a physical memory with a description of an electronic circuit design.

Accordingly, *Bayoumi* does not disclose "creating the lookup table, the lookup table having a total number of entries that is greater than or substantially equal to an upper limit, the

lookup table representing the physical memory with a description of the electronic circuit design," as recited in claim 23. Because *Bayoumi* does not disclose each of the limitations of claims 23, Applicant asserts that claim 23 is patentable over the cited art and respectfully requests withdrawal of the rejection of claim 23 under 35 U.S.C. § 102(b).

VI. Rejection of claims 24-28 under 35 U.S.C. § 103(a)

Claims 24-28 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Bayoumi* in view of *Weems*. Because *Bayoumi* and *Weems*, either alone or in combination, fail to teach or suggest each of the limitations of claims 24-28, Applicant asserts that claims 24-28 are patentable over the cited art.

As discussed above with respect to claim 23, *Bayoumi* fails to teach or suggest "creating the lookup table, the lookup table having a total number of entries that is greater than or substantially equal to an upper limit, the lookup table representing the physical memory with a description of the electronic circuit design." As previously discussed with respect to claims 1 and 14, *Weems* fails to teach or suggest a lookup table or memory model used to represent a physical memory with a description of an electronic design. Accordingly, *Weems* fails to cure the deficiency identified in *Bayoumi* with respect to the above limitation of claim 23. Additionally, nothing within the combination of these two references suggests the use of a "lookup table representing the physical memory with a description of the electronic design," as recited in claim 23. *Bayoumi* and *Weems*, respectively, are directed to developing the layout of a memory module for storing lookup tables used in RNS structures and to traditional memory caching techniques. Nothing within the combination of the references suggests representing a physical memory with a description of an electronic design using a lookup table.

Since claims 24-28 each ultimately depend from claim 23, Applicants assert that claims 24-28 are patentable for at least the reasons set forth with respect to claim 23. Accordingly, Applicant respectfully requests withdrawal of the rejection of claims 24-28 under 35 U.S.C. § 103(a).

VII. Conclusion

Based on the above amendments and these remarks, reconsideration and allowance of claims 1-44 is respectfully requested. Applicants also request consideration and allowance of new claims 45-51.

The Examiner's prompt attention to this matter is greatly appreciated. Should further questions remain, the Examiner is invited to contact the undersigned attorney by telephone.

The Commissioner is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 501826 for any matter in connection with this document, including any fee for extension of time, which may be required.

Respectfully submitted,

Date: 12/2/03

By: _____
David E. Cromer
Reg. No. 54,768

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ATTACHMENT A

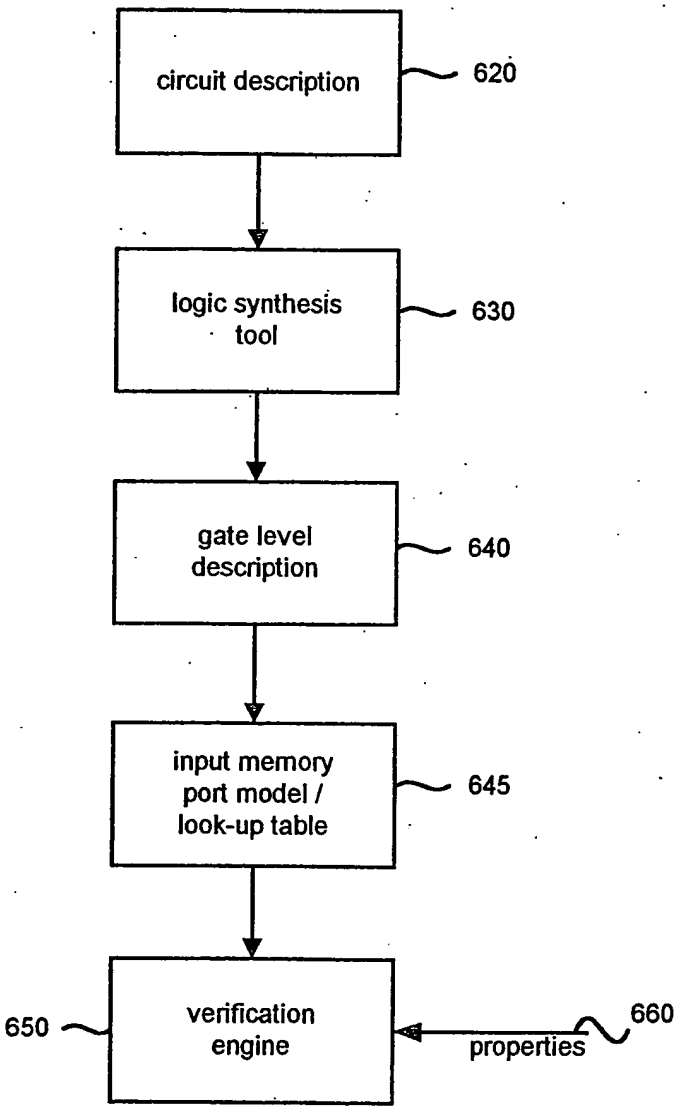

FIG. 6

ATTACHMENT B

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

COPY

In re Application		PATENT APPLICATION
Inventor(s):	Adrian J. Isles	
SC/Serial No.:	Unknown	
Filed:	Herewith	
Title:	CIRCUIT-LEVEL MEMORY AND COMBINATIONAL BLOCK MODELING	

CERTIFICATE OF MAILING BY "EXPRESS MAIL" UNDER 37 C.F.R. §1.10

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Johann S. Mercado
Signature Date: June 2, 2000

UTILITY PATENT APPLICATION TRANSMITTAL LETTER UNDER 37 C.F.R §1.53(b)

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Washington, DC 20231

Sir:

Transmitted herewith for filing is the patent application identified as follows:

Inventor: Adrian J. Isles

Title: CIRCUIT-LEVEL MEMORY AND COMBINATIONAL BLOCK MODELING

No. of pages in Specification: 41; No. of Claims: 44.

No. of Sheets of Drawings: 8 ; Formal: X , Informal: _.

Attorney Docket No.:HDAC1003US0
jav/hdac/1003/1003.002.doc

Also enclosed are:

__ A Declaration.

__ An Assignment and Recordation Form Cover Sheet.

__ A certified copy of a priority application.

__ A Power of Attorney.

__ A Statement Claiming Small Entity Status.

__ An Information Disclosure Statement under 37 C.F.R. §1.56.

The filing fee pursuant to 37 C.F.R. §1.16 is determined as follows:

	No. Filed		No. Extra		Rate Small Entity/ Other Than Small Entity		
Basic Fee					$345.00 $690.00	=	$
Total Claims	44 - 20	=	24*	X	$ 9.00 $ 18.00	=	$
Independent Claims	7 - 3	=	4*	X	$ 39.00 $ 78.00	=	$
First Presentation of Multiple Dependent Claim(s)	__				$130.00 $260.00	=	$
					Total	=	$

*If the difference is less than zero, enter "0".

__ Please charge Deposit Account No. 06-1325 in the amount of $___. A duplicate copy of this authorization is enclosed.

__ A check in the amount of $___ to cover the filing fee ($___), and assignment recording fee ($40.00), if applicable, is enclosed.

— The Commissioner is hereby authorized to charge underpayment of any additional fees (including those listed below) or credit any overpayment associated with this communication to Deposit Account No. 06-1325. A duplicate copy of this authorization is enclosed.

— Any additional filing fees under 37 C.F.R. §1.16.

— Any patent application processing fees under 37 C.F.R. §1.17.

This application is filed pursuant to 37 C.F.R. §1.53(b) in the name of the above-identified Inventor(s).

— This application claims priority to an earlier-filed Provisional patent application, as set forth more fully in this application.

Please direct all correspondence concerning the above-identified application to the following address:

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Telephone: (415) 362-3800

Respectfully submitted,

Date: June 2, 2000

By: _____
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ATTACHMENT C

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The U.S. **PATENT** Office date stamp and Serial No. (if a new application) sets forth the date of receipt of:

Applicant: Adrian J. Isles

Patent/Serial No.: _____ Issued/Filing Date: _____

Title: CIRCUIT-LEVEL MEMORY AND COMBINATIONAL BLOCK MODELING

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Pages in Spec. 41 : No. of Claims 44

☐ CPA ☐ CIP ☐ CON ☐ DIV ☐ Provisional

☑ No. of Sheets of Drawings 8 : ☒ Formal or ☐ Informal

☐ Preliminary Amendment

☐ Response to Notice of Missing Parts

☐ Assignment and Cover Sheet

☐ Declaration

☐ Power of Attorney

☐ Small Entity Statement

☐ Petition for Extension of Time (_____ months)

☐ Response

☐ FEE: $ _____

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